# Proposed Pinout for FE-I Chips

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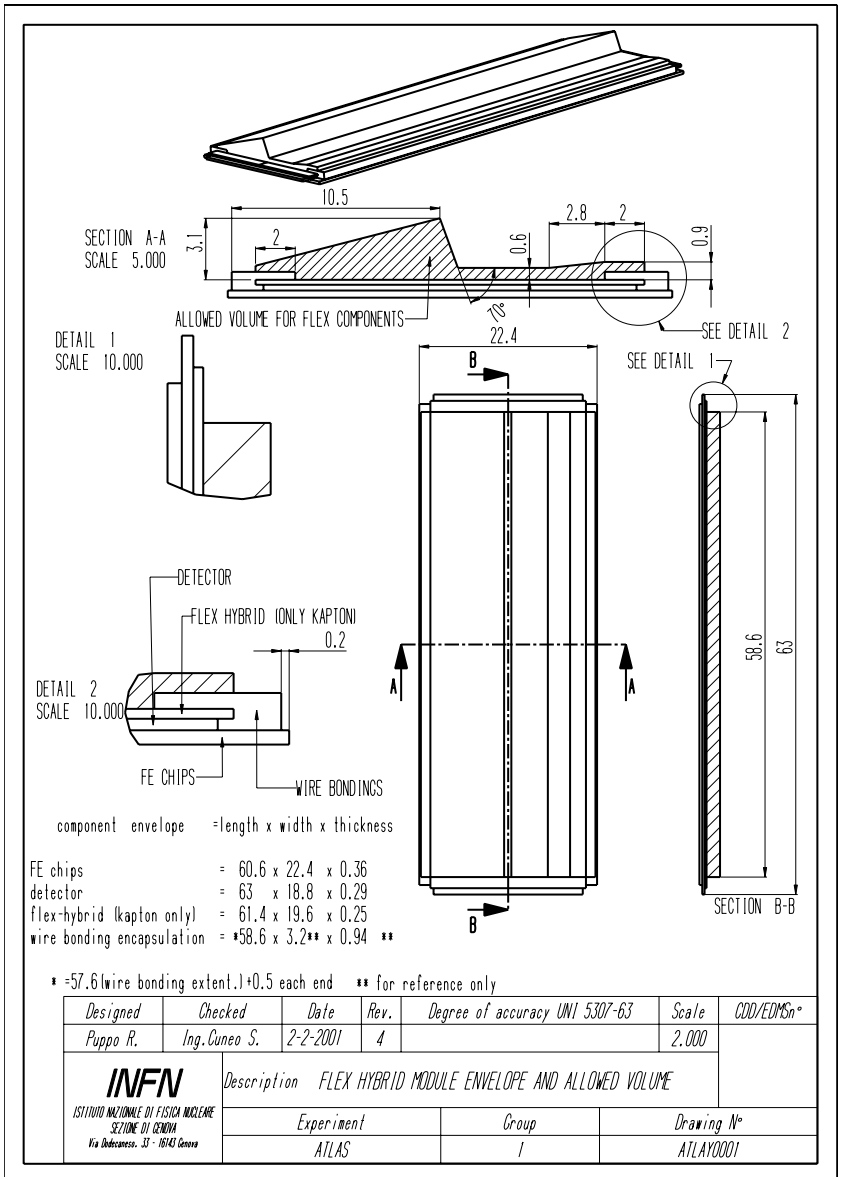
## Geometry and Pinout issues:

- Need to match production pinout and geometry to proposed module envelope.

## Propose final pinout, satisfying these constraints

# Overview of Module Envelope

## Summarize constraints on module envelope:




Constraints on FE die size:

- Present prototypes use: 7.2x(8.0+2.8)mm design size with 0.1mm dicing zone all around: 7.4x11.0mm as-cut die size.
- Production size agreed to be same: Provides total chip envelope in z of 8*7.4 + 7*0.2 = 60.6mm

Constraints on FE bonding region:

- End chips have a constraint on the region which may be wire-bonded, in order to provide good Z overlap. Bonds must fit in central 57.6mm of module, meaning central 4.4mm out of the 7.4mm as-cut die width.
- If we retain the present 150μ bond-pad spacing, that corresponds to 30 bonding pads (4.35mm + pad size).



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# Proposed Final FE Chip Pinout (30 bonded pads):

- Total of 10 power pins, positioned at 1/4 and 3/4 points in die (mirrored) :

  **p11, p38 VDDA**
  **p12, p37 AGnd**
  **p13, p36 Shield**
  **p14, p35 DGnd**
  **p15, p34 DVdd**

- Total of 1 analog pin (intended largely for lab calibration at this time):

  **p20 VCal**

- Total of 9 Command and Address pins (GA closer to DGnd):

  **p16 - p19 GA0 - GA3**
  **p21 CCK**
  **p22 DI**
  **p23 LD**
  **p32, p33 STRn, STRp**

- Total of 6 control pins (all LVDS pins are grouped together):

  **p26, p27 SYNCn, SYNCp**
  **p28, p29 XCKn, XCKp**
  **p30, p31 LV1n, LV1p**

- Total of 2 output pins (now located in chip center for easier Flex routing)

  **p24, p25 DOn, DOp**

- Total of 2 detector pins:

  **p10 DGuard**
  **p39 DGrid**

# To reach this, have removed 18 pads from present pinout:

- RSTb, and Analog pins (I1-I8, and VCCD/VTH)
- All monitoring pins (MonHit, MonSel, MonRef, MonAmp)
- Propose to retain most on the die, in locations compatible with present floorplans:
- Total of 1 control pin:

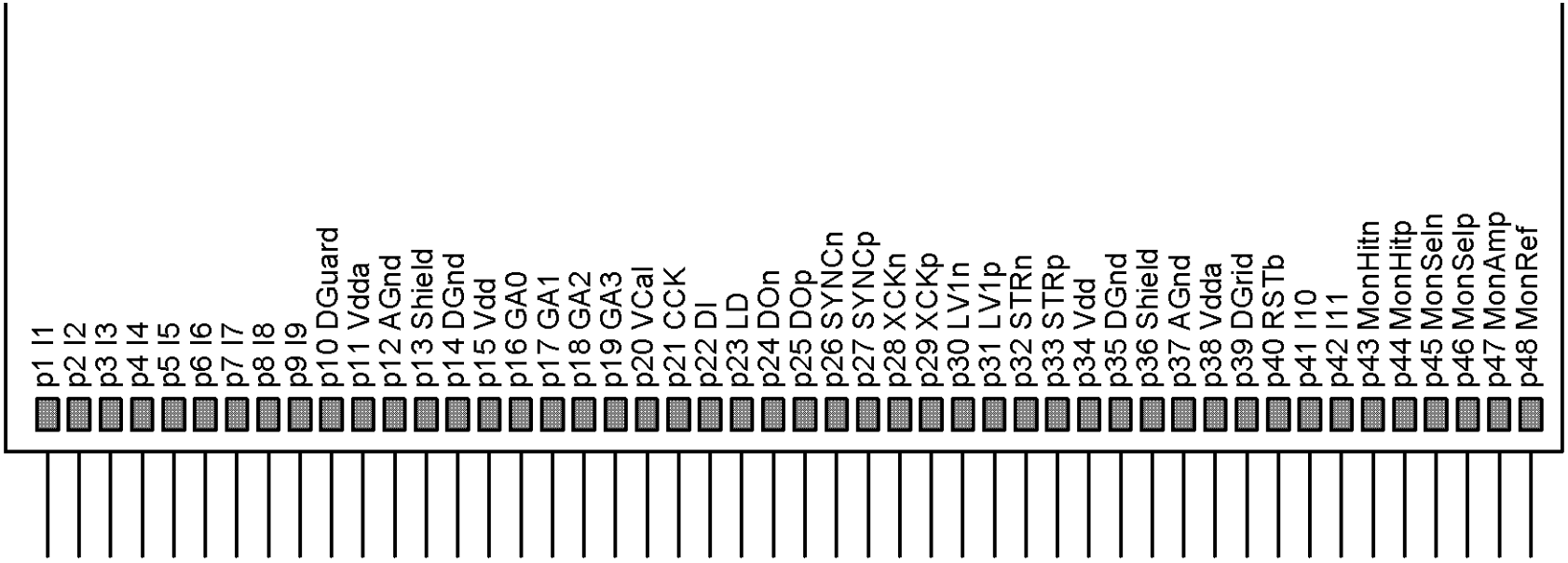
  **p40 RSTb**
- Total of 11 current monitor pins (may not all be used):

  **p1 I1**
  **p2 I2**
  **p3 I3**
  **p4 I4**
  **p5 I5**
  **p6 I6**
  **p7 I7**
  **p8 I8**
  **p9 I9**
  **p41 I10**
  **p42 I11**
- Total of 6 special monitoring pins:

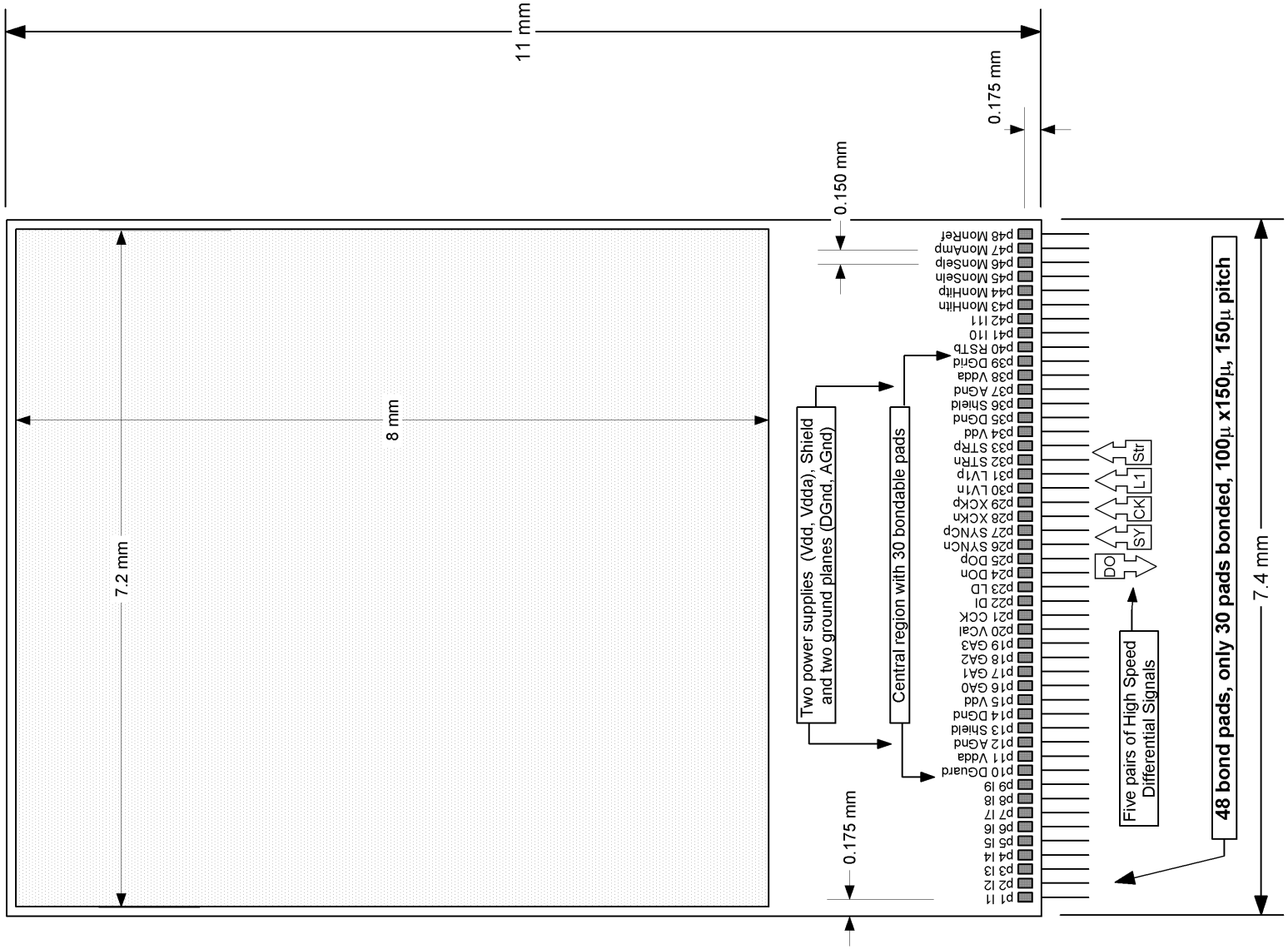
  **p43, p44 MonHitn, MonHitp**
  **p45, p46 MonSeln, MonSelp**
  **p47 MonAmp**
  **p48 MonRef**

# Proposed Pad Geometry:

- Increase present pad size to 100μ x 150μ rectangle, with 150μ pitch, to provide more pad area for rebonding. Include MCM-D bump-bondable I/O pads with the same geometry used in FE-D (relative to the bottom of the wire bond pads).
- Continue to locate pads close to the lower die edge, as for demonstrator chips.
- The present demonstrator geometry has 48 pads, with centers along a line 175μ above the bottom (referenced to the as-cut die size of 7.4x11.0mm). The first pad center is also 175μ from the vertical edge referenced to the as-cut die size.
- Propose that this pad placement would be retained, and only the central 30 pads would be used for production bonding:



# Overall Chip Geometry:



# Status of this Proposal:

- This proposal has been discussed with FE design community, and has been presented and discussed during the Feb Pixel week in the Flex and Module meetings.
- Minor modifications to the original proposal were made, and this should now be the final draft of the proposal.
- Further modifications in the non-bonded pads could still be considered.
- It will be circulated one more time, and then considered approved for the FE-I design and the Flex 3 designs.
- Probe card design based on this pinout should also begin soon in order to prepare for the arrival of the new chips.